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Orientation dependence of the charge distribution and quantum capacitance in silicon nanowire transistors

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Orientation dependence of the charge distribution and quantum capacitance in silicon nanowire transistors

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Abstract

CMOS devices are evolving from planar to 3D non-planar devices at nanometer scale to meet the ITRS [1] scaling requirements. These devices will operate under strong confinement and strain, regimes where atomistic effects are important. This work focuses on the quantum effects on the electrostatics of ultra-scaled silicon nanowire transistors. The method is based on the calculation of nanowire dispersion using an atomistic tight-binding (TB) model (sp3d5s* -SO) coupled self-consistently to a 2D Poisson equation solver. We enable the understanding of atomistic treatment in the charge distribution as well as the capacitance measurements in these ultra-scaled silicon nanowire transistors. This work will enhance the already available Bandstructure Lab tool on nanoHUB.org.

Introduction – Approach

The 2D cross section of a 3D device is described with an arbitrary geometrical shape such as rectangular, cylindrical and triangular gate all around type of structures (Fig. 1(a-d)). A finite element mesh enables the treatment of extended device components (green color) and includes the atomic locations in the interior semiconductor (red dots). The electronic structure in a nanowire channel is described in an atomistic representation using a 20 orbital nearest-neighbor tight binding model with spin orbit coupling ($sp^3s^*d^5$-SO) [2]. A nanowire with a given cross section and transport orientation is specified, and its corresponding bandstructure is calculated using the unit cell information, based on the underlying atomic lattice (Fig. 1e). To account for any changes to the bandstructure due to potential and charge variations in the wire, the electronic structure is calculated self-consistently coupled to a Poisson solver for the electrostatic potential in the cross section (Fig. 1f). Upon potential convergence of the infinite wire, the ballistic transport characteristics are calculated using a semi-classical ballistic model (Fig. 1g) [3].

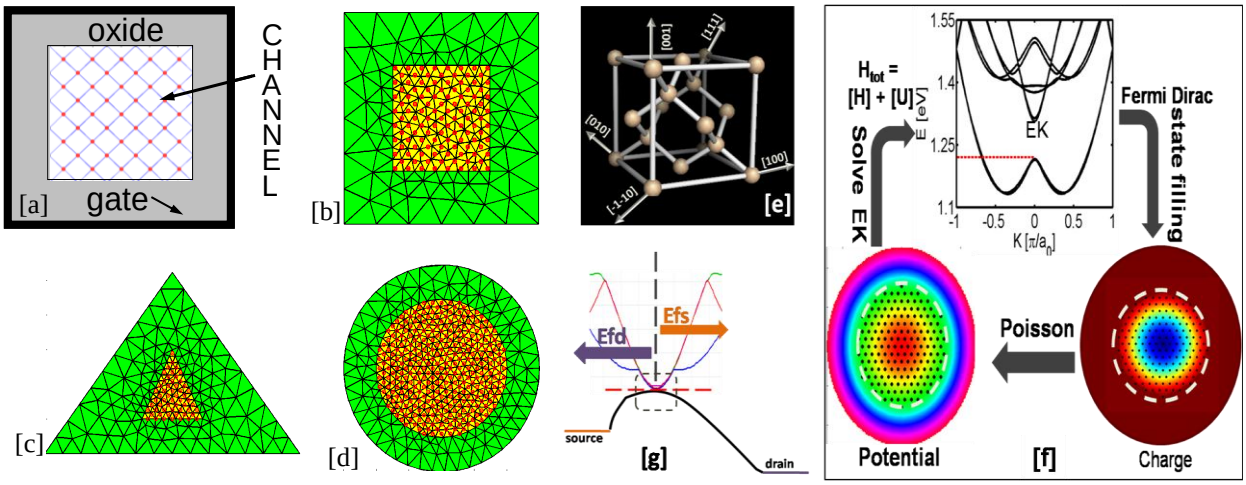

Figure 1: [a] Structure of nanowire transistor with atomistic core and continuum gate oxide around it. [b-d] Various cross-section geometries (rectangle, triangle and circle respectively) that are solved by the tool with finite element mesh for Poisson solution. Green region is the oxide and red dots are the atoms making the semiconductor core.
[e] Underlying atomistic zinc-blende unit cell used for creating nanowire transistor core. [f] Self-consistent simulation procedure. [g] Top of the barrier ballistic transport model.

Results – Discussion

Spatial inversion charge distribution in nanowires has a strong dependence on wire transport direction. Figure 2 and 3 show inversion electron distribution in smaller (3nm) and larger (5nm) rectangular cross-section silicon nanowires

for three different orientations with 1nm silicon dioxide all around. The spatial distribution of electron charge is observed to be governed mainly by, (i) the cross-section shape of wire, (ii) orientation of the wire surface (transport direction) and (iii) cross-section size of wire. This work focuses on the factors (ii) and (iii). Under inversion the 1D electron charge density, N^{1d}_{inv} (per unit length) is given by,

$$N^{1d}{}_{inv}(x,y) = 2\sum_i \sum_j \psi^*_{ji}\psi_{ji} \times [1+\exp((E_{fs}-E^i_j)/KT)]^{-1}$$
$$= 2\sum_i \sum_j [1+\exp((E_{fs}-E^i_j)/KT)]^{-1} \,|\psi_{ji}(x,y)|^2 \quad \text{---- (1)}$$

where T and K are device temperature and Boltzmann's constant. Indices *i* and *j* run over the number of sub-bands and k points per sub-band in 1D dispersion of a nanowire, respectively. E_{fs} and E^i_j are the source Fermi level and j_{th} eigen energy value of i_{th} sub-band respectively.

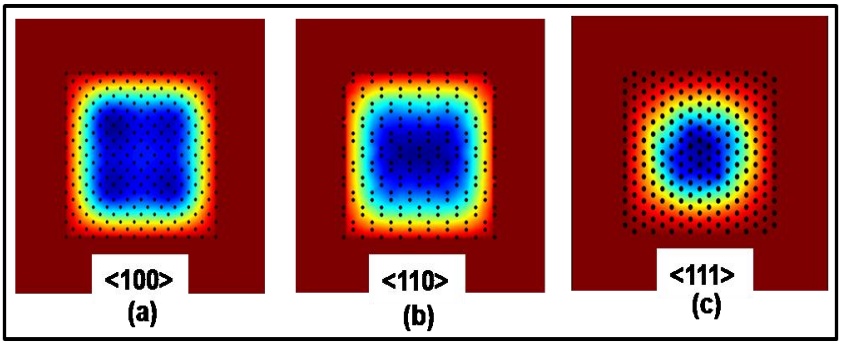

Figure 2: Spatial distribution of electrons under high Vg in a 3.1nm X 3.1nm rectangular silicon nanowire with 1nm SiO_2 all around. [100] and [110] wires push the charge towards the periphery, but not very pronounced due to smaller cross section size. [111] wire has central charge distribution.

The value of 2 in front (eqn.1) only needs to be included if spin is neglected in the sp3d5s* basis, which is an acceptable assumption for the electrons in Silicon. For holes, however, or for narrow-gap materials spin should not be neglected and can be directly included in the sp3d5s* basis. *Ψji(x,y)* is the confined plane wave (eigen) function obtained from the unitcell TB hamiltonian of the wire. The square of the absolute value of the eigen functions ($|\Psi ji(x,y)|^2$) determines the nature of spatial charge distribution in the confined plane. The filling of conduction band states is controlled by the position of 1D dispersion and the Fermi level (E_{fs}) as reflected from Eq. 1.

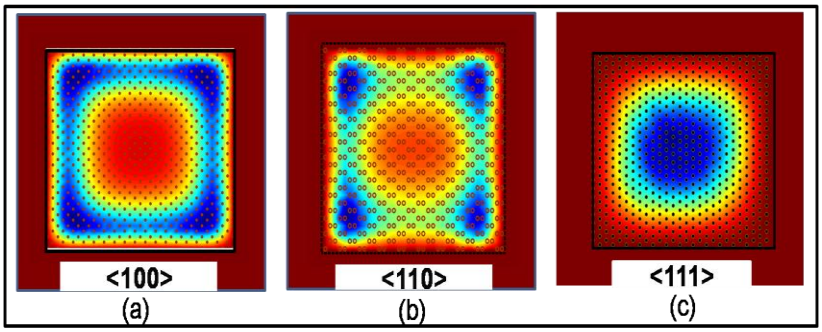

Figure 3: Spatial distribution of electrons under high Vg in 5nm rectangular silicon nanowire with 1nm SiO2 around. In [100] and [110] wire, charge moves to the corners, where as it is confined at the center in [111] wire.

The Γ (green circle) and/or the off-Γ (red circle) valley(s) (Fig. 4) play a crucial role in determining the amount of charge filled in these nanowires. From Eq. 1 it becomes clear that the nature of eigen functions at these valleys will dominate the charge distribution pattern in the wires since these valleys are first filled by E_{fs}. From fig. 4a we can observe that for [100] wire Γ is the dominating valley (closest to E_{fs}) compared to the off-Γ valley. Therefore, charge distribution takes the pattern governed by the eigen state at Γ valley. The first two sub-bands provide eigen states that are well spread to the corners (fig. 5a). The less influential off-Γ valley has spherically symmetrical eigen states (fig. 5b). This kind of eigen state distribution pushes the charge equally along x-y axis of the confined plane (fig. 2a). For a larger cross-section wire the electrostatic corner effect further spreads the charge as a result of which corners are inverted more compared to the edges (fig 3a).

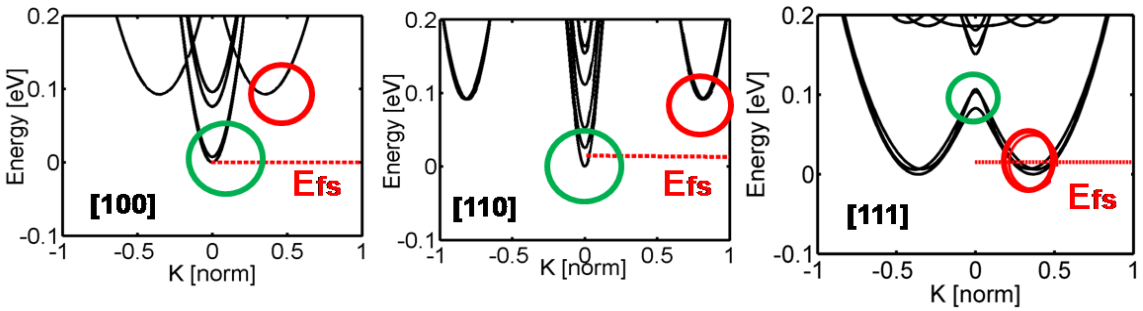

Figure 4. 1D dispersion of a 3.1nm X 3.1 nm rectangular nanowire at a gate bias of 0.8 V for three different confined surfaces [a] [100] [b] [110] & [c] [111]. Green circle show the Γ valley and red circle show the off-Γ valley. Red dotted line is the source Fermi level (E_{fs}).

In case of [110] wire the first two eigen states at the Γ valley have a preferential spread towards y direction in the confined plane while the off-Γ valley eigen state is quite symmetric with slight spreading towards y direction. The result of such eigen state distribution in [110] wire invert the channel more along the y axis compared to x axis (fig. 2b). In larger cross-section wires this *y* direction inversion is coupled with corner effect and as a result 4 distinct inverted regions appear at the corners, while the edges are not equally inverted (fig 6b). In case of [111] wires the off-Γ valley is closer to the Fermi-level compared to the Γ valley (fig.4c) The eigen states at the off-Γ valley play a major role in deciding the electron distribution. First two eigen states at the off-Γ valley are strongly confined at the center (fig. 5f) and this causes the charge to be at the center (fig 2c). Γ valley eigen states have a preferential x direction shift (fig. 5e), however, they are quite far above the Fermi-level and hence are empty, thereby not affecting the electron distribution too much. When the cross-section becomes larger still due to the strong confinement of the wave functions at the center, the channel is more inverted at the center rather than at the corners or edges (fig 3c).

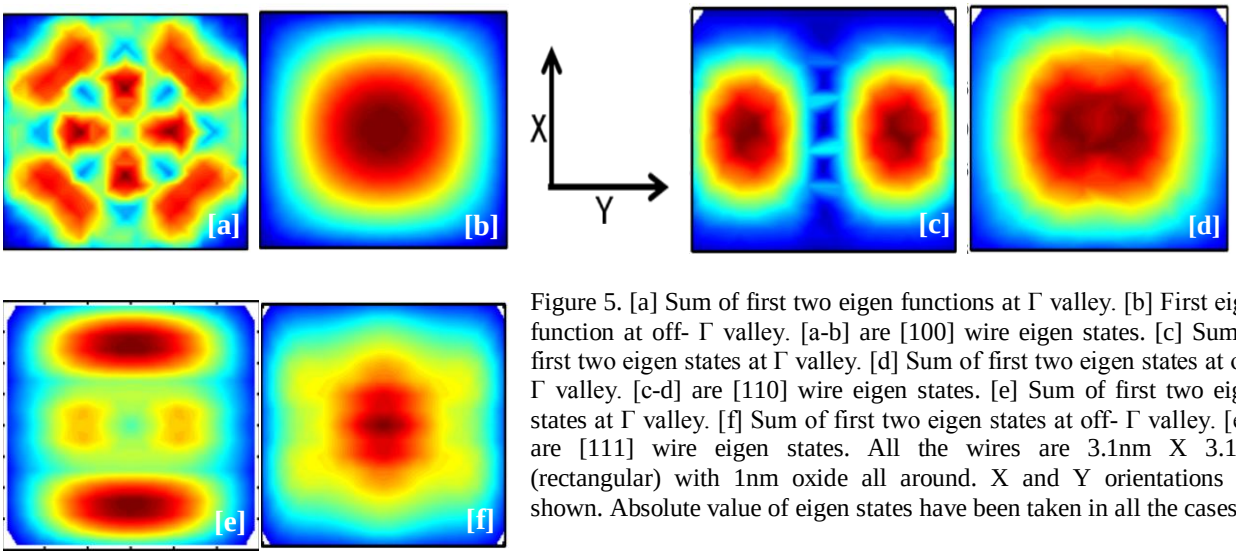

Figure 5. [a] Sum of first two eigen functions at Γ valley. [b] First eigen function at off- Γ valley. [a-b] are [100] wire eigen states. [c] Sum of first two eigen states at Γ valley. [d] Sum of first two eigen states at off-Γ valley. [c-d] are [110] wire eigen states. [e] Sum of first two eigen states at Γ valley. [f] Sum of first two eigen states at off- Γ valley. [e-f] are [111] wire eigen states. All the wires are 3.1nm X 3.1nm (rectangular) with 1nm oxide all around. X and Y orientations are shown. Absolute value of eigen states have been taken in all the cases.

Quantum capacitance (Cq) calculations give a direct evidence of change in DOS near the Fermi level. Cq is, however, not a constant but shows large changes as the Fermi-level (E_{fs}) is pushed inside the conduction bands (Ec). In fig. 6 large swings in Cq are quite evident and it can be correlated directly to the position of the Fermi-level inside Ec.

$$g_{1d}(E) = \frac{1}{2\pi}\left(\partial E / \partial K\right)^{-1} \quad \text{---- (2)} \qquad C_g = C_{ox}C_s/(C_{ox}+C_s) \quad \text{--- (3)} \qquad C_s = C_q\left(1-\frac{\partial E_i}{\partial \varphi_s}\right) \quad \text{--- (4)}$$

At the bottom of any conduction band the 1D DOS shoots up since dE/dK goes to zero (eq. 2) and Cq rises (Fig. 6 b–c). As E_f scans the conduction bands the 1D DOS falls and so does Cq (Fig. 6 a & d). However, for these nanowire transistors we can only measure gate capacitance (Cg). Eqn. 3 shows Cg is a series combination of oxide capacitance

(Cox) and semiconductor capacitance (Cs). Since Cox in these devices is very close to Cs, Cg does not reflect the nature of Cq , but Cg value degrades quite a bit [4]. Another reason for the Cg degradation is that Cs is related to Cq by Eq. 4 which shows how well the sub-bands move when the surface potential (φ_s) changes, which in turn is related to the gate bias (Vg). For high-K material Cox will be much larger than Cq hence the effect of Cq in Cg will be prominent. Cg degradation will be less since the electrostatic gate coupling to the channel is stronger.

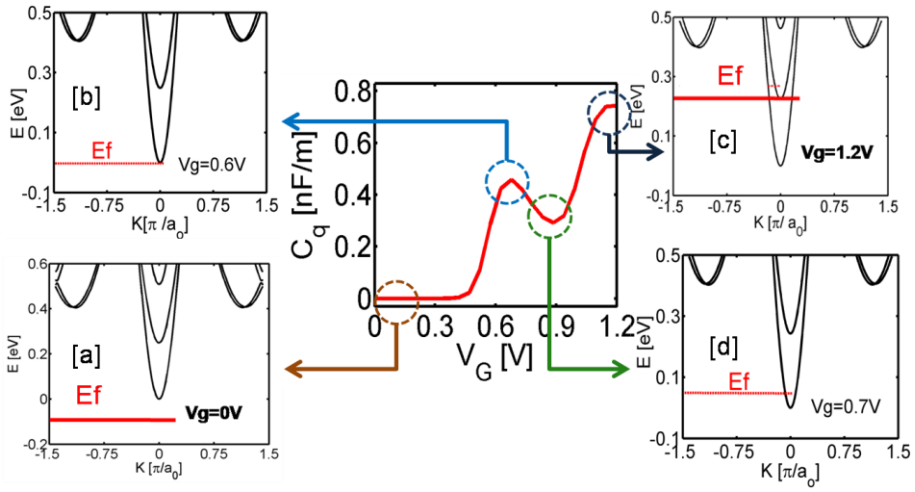

Fig. 6. Quantum capacitance (Cq) variation in a 1.5nm [110] rectangular silicon nanowire with 1.1 nm gate oxide all around. [a-d] show the position of the Fermi-level (E_{fs}) in the conduction band (E_c). Initially E_{fs} 0.15eV below the conduction band minima(Vg = 0). As Fermi level scans the sub-bands Cq increases and decreases which is directly correlated to the change in 1D-DOS around E_{fs}. E_f is also the Fermi level.

Conclusion

The atomistic TB model provides a generic way to handle nanowires of different orientations and capture the quantum effects and full-band interactions in ultra-scaled semiconductor devices which govern their electrostatic properties. Not shown here is that strain can be included naturally by bond distortions which modify the local band structure. [100] and [110] wires are direct band-gap devices compared to [111] wire which is indirect band-gap. The nature of the eigen states around certain valleys govern the overall electron distribution in wires. Corner effects are confirmed to be dominant in larger cross-section wires [5]. As the wire cross-section increases different regions of wires are preferentially inverted which will affect the device threshold voltage (V_{th}) and hence the device properties at the circuit level. The nature of the quantum capacitance in these nanowire devices can be well understood by the full band treatment. Under strong geometrical and electrostatic potential confinement the sub-bands get separated and as a result changes in 1D-DOS can be directly correlated to the Fermi level position inside the conduction band. These features may or may not show up at the terminal capacitance measurement depending on the size of the wire as well as the kind of gate insulator used in these devices. Low temperature measurements are expected to resolve the charge variations. The model used in this work has been integrated as an enhancement to the existing Banstructure Lab tool [6] on nanohub.org which is open for public use.

Acknowledgements

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References

[1] ITRS Public Home Page. http://www.itrs.net/reports.html.
[2] G. Klimeck, F. Oyafuso, T. B. Boykin, R. C. Bowen, and P. von Allmen, *Computer Modeling in Engineering and Science (CMES)*, vol. 3, no. 5, pp. 601-642, 2002.
[3] A Rahman *et. al*, "Theory of Ballistic nanotransistors", IEEE TED, 50, pp. 1853-1864, 2003.
[4] N. Neophytou, A Paul, M Lundstrom and G. Klimeck, "Bandstructure effects in silicon nanowire transistors", to appear in IEEE TED, Vol 55 –no.6, June 2008
[5] Ruiz et. al, "A comprehensive study of the corner effects in pi-gate mosfets including quantum effects", IEEE TED, Vol 54 –no. 12, Dec. 2007
[6] See http://www.nanohub.org/tools/bandstrlab/ for the deployed Bandstructure Lab. Source code management of the latest Bandstructure Lab V2.0 on nanoHUB.org (https://developer.nanohub.org/projects/app-bstr_sc_lab).